IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

ARBOR GLOBAL STRATEGIES LLC, a Delaware Limited Liability Company,	)	
Plaintiff,	)	C.A. No.
v.	)	
	)	**DEMAND FOR JURY TRIAL**
XILINX, INC., a Delaware Corporation,	)	
Defendant.	)	

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Arbor Global Strategies LLC ("Arbor") files this Complaint for Patent Infringement and Demand for Jury Trial against defendant Xilinx, Inc. ("Defendant" or "Xilinx") and alleges as follows:

THE PARTIES

1. Arbor is a Delaware corporation engaged in the electronics and computer industry and with its principal place of business in Glenbrook, Nevada. Arbor developed and holds patents directed to novel aspects of integrated circuit ("IC") technology, including the ability to increase the amount and speed of connections within an IC module. This patented IC technology has important applications, particularly in devices with restricted form factors, such as in modern smartphones and tablets.

2. Mr. D. James Guzy is the Chairman, President, and Co-founder of Arbor and has been with the parent company of Arbor since 1969. Mr. Guzy is an acknowledged pioneer in Silicon Valley, co-founded the Intel Corporation, was Intel's longest serving director, and has served in various senior and advisory capacities in several other technology companies. Mr.

Guzy has a MS from Stanford University, a BS from University of Minnesota, and is one of the inventors on Arbor's patents.

3. Xilinx is a corporation incorporated under the laws of Delaware, having its principal place of business at 2100 Logic Drive, San Jose, CA 95124. Xilinx's registered agent for service of process in the State of Delaware is The Corporation Trust Company, Corporation Trust Center, 1209 Orange Street, Wilmington, Delaware 19801.

4. On information and belief, Xilinx has been engaged in the business or manufacturing, using, offering for sale, and/or selling in the United States, and/or importing into the United States, integrated circuit ("IC") products that utilize Field-Programmable Gate Array ("FPGA"), and these ICs include the use of through-silicon vias ("TSVs") within an IC, such as between multiple die layers or components that include at least one FPGA.

JURISDICTION AND VENUE

5. This action arises under the Patent Act, 35 U.S.C. § 101 *et seq*. This Court has original jurisdiction over this controversy pursuant to 28 U.S.C. §§ 1331 and 1338.

6. This Court has personal jurisdiction over Defendant in this district, in that Defendant, directly or through its agents, is a resident of, and/or has regularly conducted business activities in this district; has committed infringing activities in this district by manufacturing, using, marketing, offering for sale, selling and/or importing products and systems that infringe Arbor's patents, and/or has placed products and systems that infringe in the stream of commerce with the knowledge and intent that they would be used, offered for sale and/or sold by others in this district.

7. Venue is proper in this Court pursuant to 28 U.S.C. §§ 1391(b) and (c) and/or 1400(b).

ARBOR'S INNOVATIONS

8. Arbor pioneered and developed novel IC technologies, for which it holds several patents. The innovations in these patents relate to a new type of IC called a "stacked die hybrid," which allows for an extremely compact processor module with increased data speeds and processing efficiency. These inventions also include the use of TSVs within an IC module, such as between die layers or components. This novel use of TSVs provides for increased bandwidth and efficiency as well as a smaller form factor than allowed for by traditional IC fabrication techniques.

9. As explained in the specification of Arbor's patents, prior art approaches to IC module design connected die layers using metallization contacts at the edges of the die. This prior art approach provided fewer and slower connections than are possible with the use of TSVs as developed by Arbor, which also improved system bandwidth and reduced power requirements.

10. Arbor's inventive use of TSVs in processor modules is particularly valuable with Field Programmable Gate Arrays (FPGA) IC modules in order to allow for high bandwidth and low latency operation of the module. For example, High Bandwidth Memory (HBM) provides increased memory capability for data-intensive, high volume applications, but requires high bandwidth components in order to realize the capabilities and benefits of HBM. The use of TSVs allows Xilinx FPGA modules to operate at high bandwidth with HBM for various applications, such as graphics processing and machine learning.

ARBOR'S ASSERTED PATENTS

11. On August 24, 2004, the USPTO issued to Jon M. Huppenthal and D. James Guzy U.S. Patent No. 6,781,226 ("the '226 Patent"), titled "Reconfigurable Processor Module

Comprising Hybrid Stacked Integrated Circuit Die Elements." A true and correct copy of the '226 Patent is attached to this Complaint as **Exhibit 1** and is incorporated by reference herein.

12. All rights, title, and interest in the '226 Patent have been assigned to Arbor, who is the sole owner of the '226 Patent.

13. The '226 Patent is generally directed towards a module comprising stacked IC die elements constructed by stacking thinned die elements connected using TSVs. The '226 Patent discloses and specifically claims inventive concepts that represent significant improvements over conventional ICs because it results in a favorable form factor with greater parallelism, higher bandwidth and throughput, and reduced power requirements for many applications.

14. On October 24, 2006, the USPTO issued to Jon M. Huppenthal and D. James Guzy U.S. Patent No. 7,126,214 ("the '214 Patent"), titled "Reconfigurable Processor Module Comprising Hybrid Stacked Integrated Circuit Die Elements." A true and correct copy of the '214 Patent is attached to this Complaint as **Exhibit 2** and is incorporated by reference herein.

15. All rights, title, and interest in the '214 Patent have been assigned to Arbor, who is the sole owner of the '214 Patent.

16. The '214 Patent is generally directed towards a module comprising stacked IC die elements constructed by stacking thinned die elements connected using TSVs. The '214 Patent discloses and specifically claims inventive concepts that represent significant improvements over conventional ICs because it results in a favorable form factor with greater parallelism, higher bandwidth and throughput, and reduced power requirements for many applications.

17. On October 16, 2007, the USPTO issued to Jon M. Huppenthal and D. James Guzy U.S. Patent No. 7,282,951 ("the '951 Patent"), titled "Reconfigurable Processor Module

Comprising Hybrid Stacked Integrated Circuit Die Elements." A true and correct copy of the '951 Patent is attached to this Complaint as **Exhibit 3** and is incorporated by reference herein.

18. All rights, title, and interest in the '951 Patent have been assigned to Arbor, who is the sole owner of the '951 Patent.

19. The '951 Patent is generally directed towards a module comprising stacked IC die elements constructed by stacking thinned die elements connected using TSVs. The '951 Patent discloses and specifically claims inventive concepts that represent significant improvements over conventional ICs because it results in a favorable form factor with greater parallelism, higher bandwidth and throughput, and reduced power requirements for many applications.

20. On January 18, 2011, the USPTO re-issued to Jon M. Huppenthal and D. James Guzy U.S. Patent RE42,035 ("the '035 Patent"), titled "Reconfigurable Processor Module Comprising Hybrid Stacked Integrated Circuit Die Elements." A true and correct copy of the '035 Patent is attached to this Complaint as **Exhibit 4** and is incorporated by reference herein.

21. All rights, title, and interest in the '035 Patent have been assigned to Arbor, who is the sole owner of the '035 Patent.

22. The '035 Patent is generally directed towards a module comprising stacked IC die elements constructed by stacking thinned die elements connected using TSVs. The '035 Patent discloses and specifically claims inventive concepts that represent significant improvements over conventional ICs because it results in a favorable form factor with greater parallelism, higher bandwidth and throughput, and reduced power requirements for many applications.

23. The '226, '214, '951, and '035 Patents are generally directed towards a module comprising IC die elements connected using TSVs. The '226, '214, '951, and '035 Patents disclose and specifically claim inventive concepts that represent significant improvements over

conventional systems by teaching persons skilled in the art how to create and use an IC module that allows for flexible form factors and increased performance compared to what was known at the time in 2001. In particular, the '226, '214, '951, and '035 Patents disclose more than just a simple combination of generic components that are used to perform conventional activities. These patents represent a pioneering use of TSVs in FPGA IC products which has been widely adopted in the industry, particularly by Xilinx.

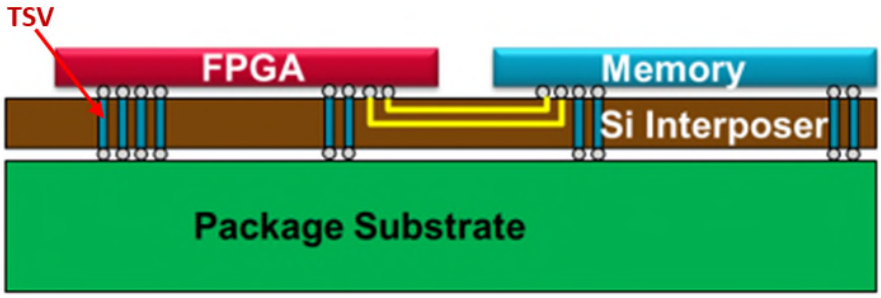
DEFENDANT'S INFRINGING PRODUCTS AND TECHNOLOGIES

24. Defendant makes, uses, sells, offers for sale, and/or imports into the United States and this District products and services that utilize Xilinx's ICs with 3D Stacked Silicon Interconnects ("SSI") and HBM, which include Xilinx's Virtex FPGA, Virtex UltraScale FPGA, Virtex UltraScale+ FPGA, Kintex UltraScale FPGA, Kintex UltraScale+ FPGA ICs, and Virtex UltraScale+ HBM ICs (collectively, the "Accused Products"). The Accused Products each include at least one FGPA in the IC module.

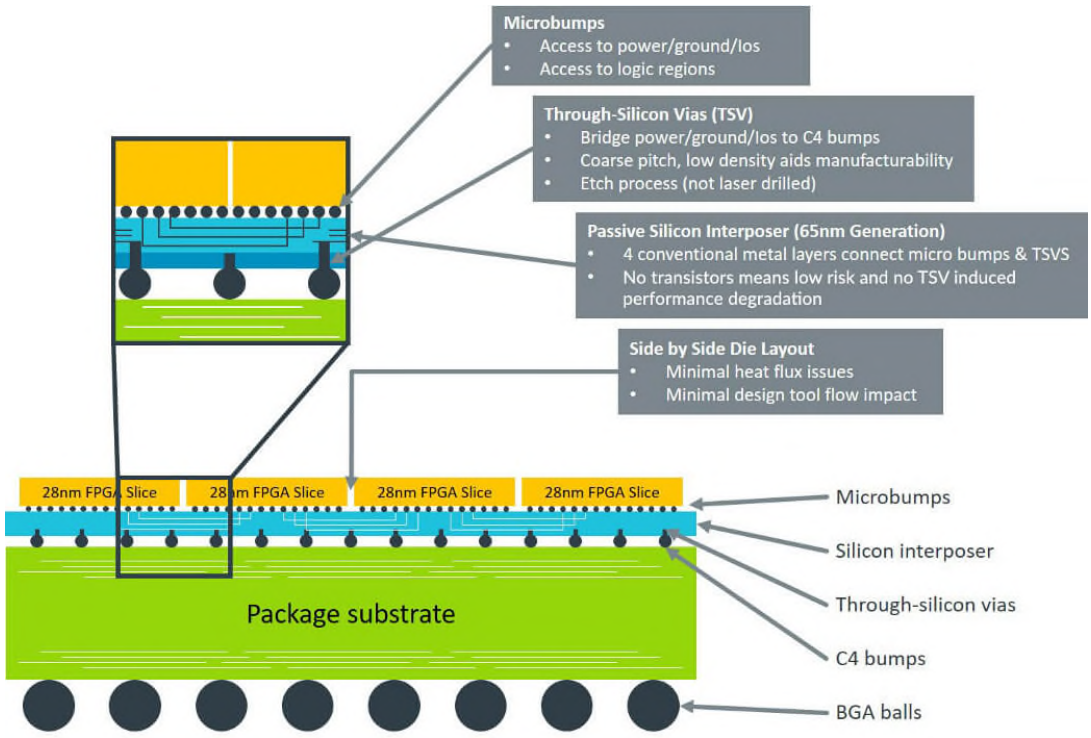
25. Xilinx's 3D ICs utilize SSI technology to enable high-bandwidth connectivity between multiple die and provide massive inter-die bandwidth-per-watt compared to the multiple chip approach.

26. As shown below, Xilinx uses 3D high-performance FPGA ICs with SSI technology. This technology leverages the use of TSVs and a silicon interposer layer to achieve

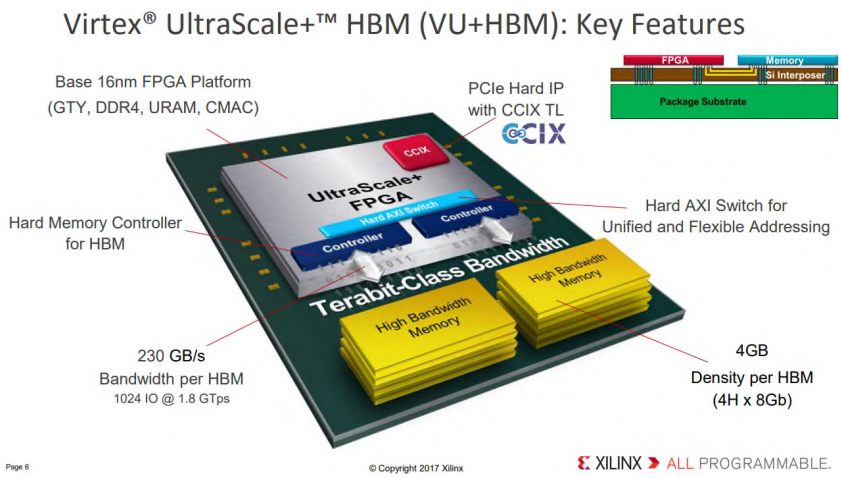
high-bandwidth and low latency connectivity between multiple heterogeneous die elements, such as between different FPGA logic die, transceivers, and memory units.



27. The Accused Products leverage microbump technologies with TSVs to deliver reliable interconnect without performance degradation on a FPGA device.



28. Xilinx's Virtex UltraScale+ FPGA products may be designed to work with HBM which, as described *supra*, requires the high bandwidth and low latency provided by the use of TSVs as taught in Arbor's Patents.



COUNT I
(Direct Infringement of the '226 Patent pursuant to 35 U.S.C. § 271(a))

29. Arbor repeats, realleges, and incorporates by reference, as if fully set forth herein, the allegations of the preceding paragraphs, as set forth above.

30. Defendant infringes at least Claim 1 of the '226 Patent in violation of 35 U.S.C. § 271(a).

31. Defendant's infringement is based upon literal infringement or, in the alternative, infringement under the doctrine of equivalents.

32. Defendant's acts of making, using, importing, selling, and offering for sale infringing products and services were without the permission, consent, authorization, or license of Arbor.

33. Defendant's infringement includes the manufacture, use, sale, importation and offer for sale of Defendant's IC products that utilize processor modules that include multiple die elements electronically coupled through TSVs, including Xilinx's ICs with 3D Stacked Silicon Interconnects ("SSI") and HBM, which include Xilinx's Virtex FPGA, Virtex UltraScale FPGA, Virtex UltraScale+ FPGA, Kintex UltraScale FPGA, Kintex UltraScale+ FPGA ICs, and the Virtex UltraScale+ HBM ICs (collectively, the "'226 Accused Products").

34. The ‘226 Accused Products practice the patented invention of the ‘226 Patent and Defendant infringes the ‘226 Patent because it makes, sells, offers for sale, and/or uses the Accused Products, which include processor modules that include multiple die elements electronically coupled through TSVs. Using the patented technology, the ‘226 Accused Products provide increased bandwidth and low latency operation.

35. The ‘226 Accused Products utilize 3D integrated circuits and SSI and are processing modules with a FPGA IC die element including programmable CLBs. Xilinx SSI technology uses the ASMBL architecture, which is a module structure including FPGA building blocks as stacked tiles.

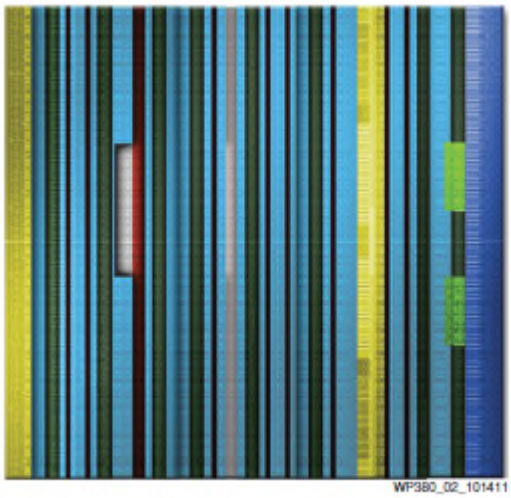


Figure 2: **Representation of an FPGA Built with ASMBL Architecture**

36. The ‘226 Accused Products include FPGA IC die elements stacked with and electrically coupled using interposers with TSVs to interconnect different logic regions.

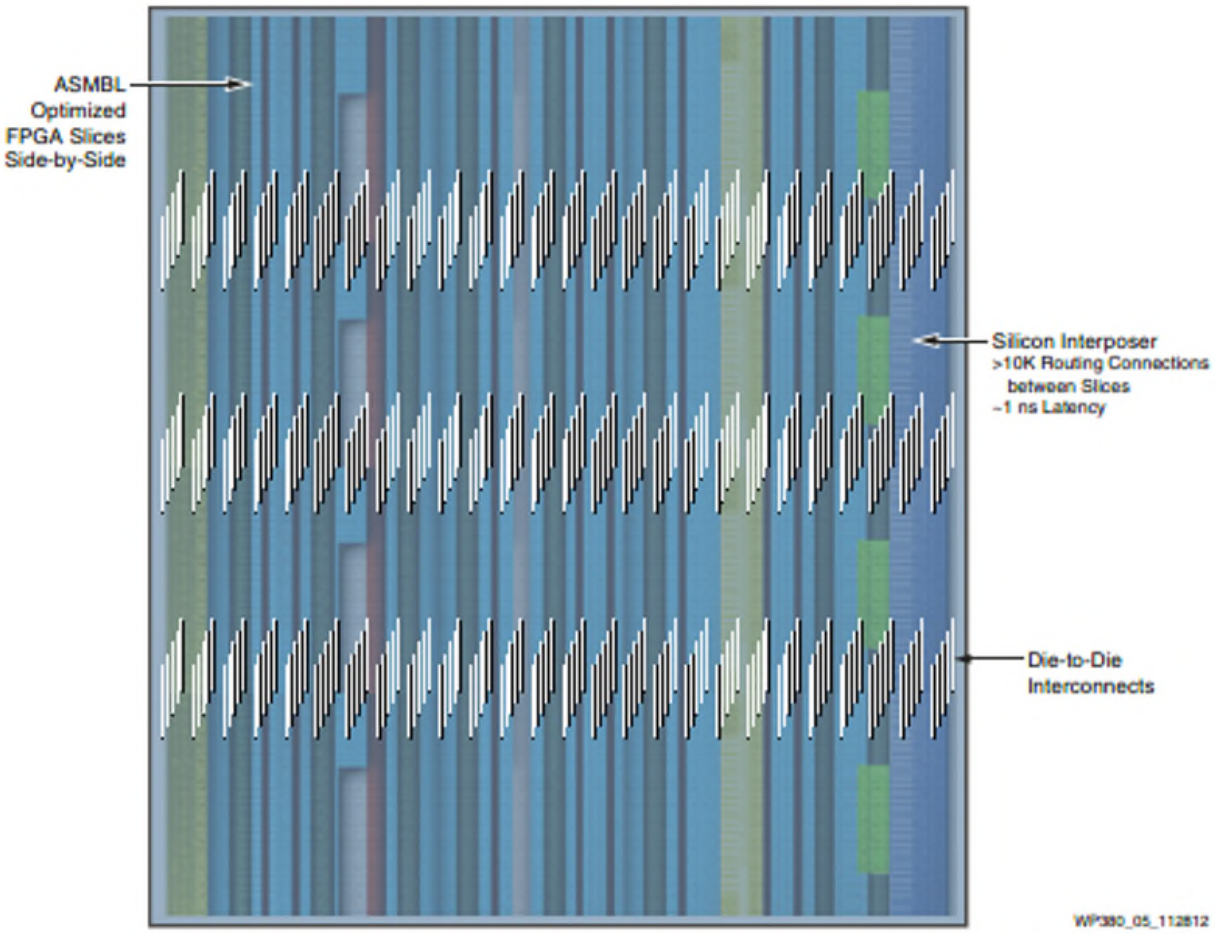
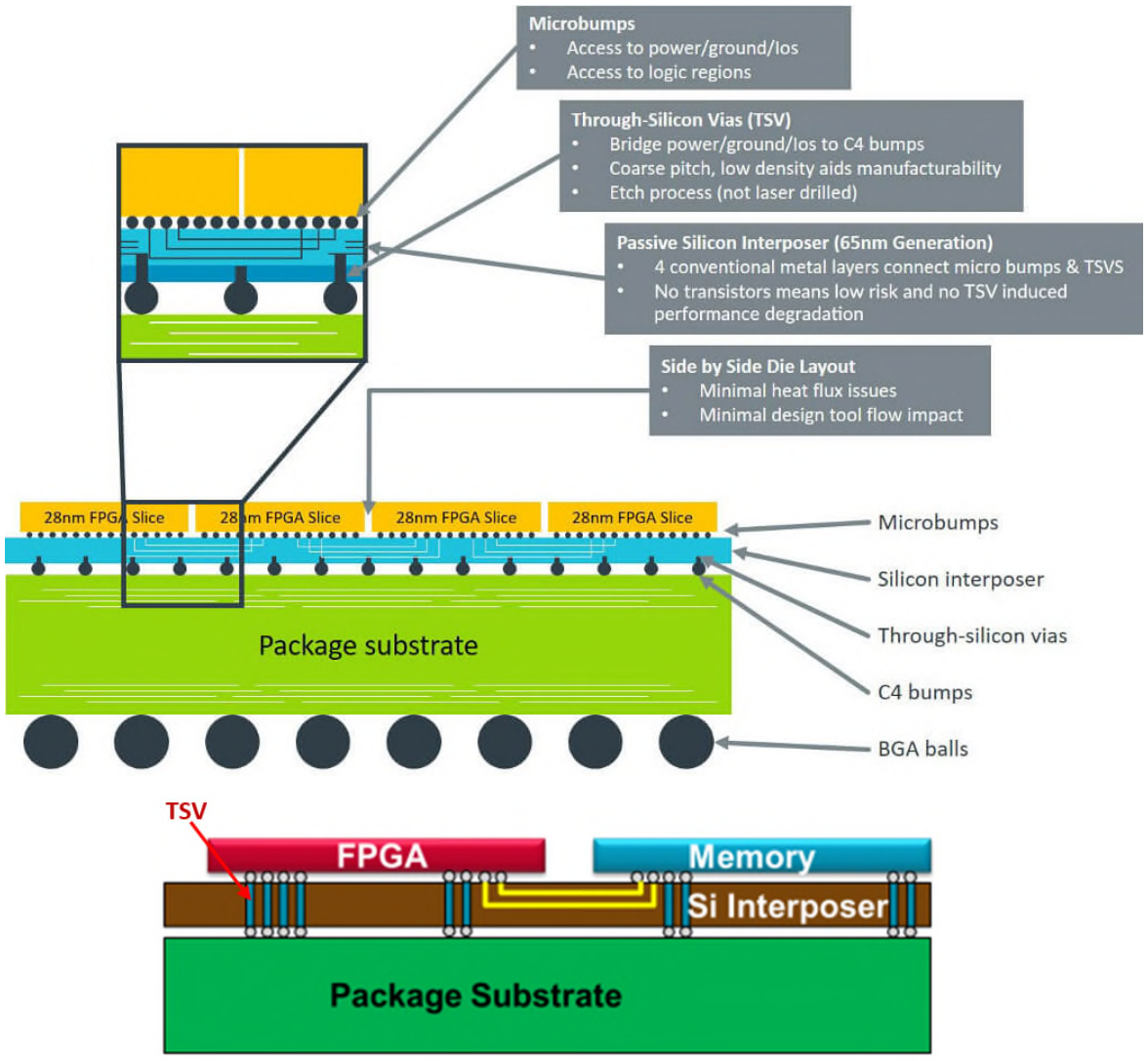


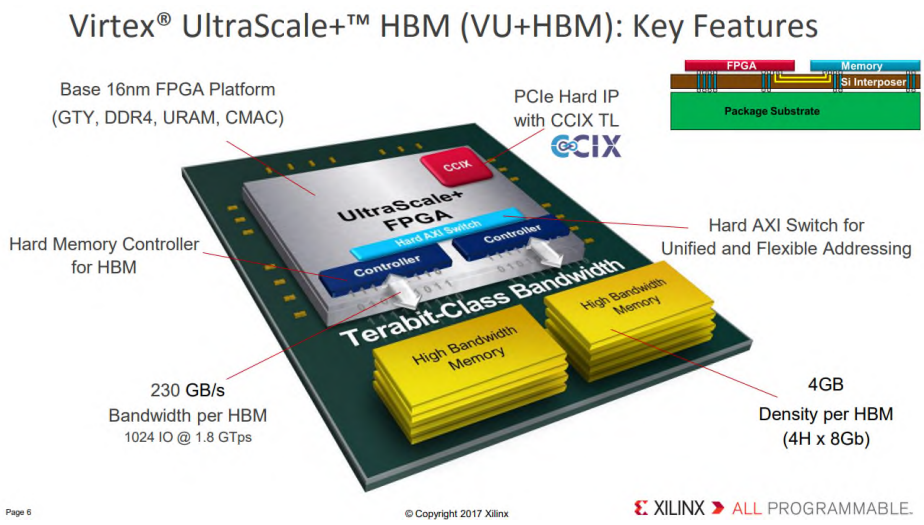
Figure 5: **"X-ray View" of a Virtex-7 FPGA Using SSI Technology**

37. Xilinx's product materials make clear that the die elements in the '226 Accused Products are electrically coupled and interconnected using interposers with TSVs.

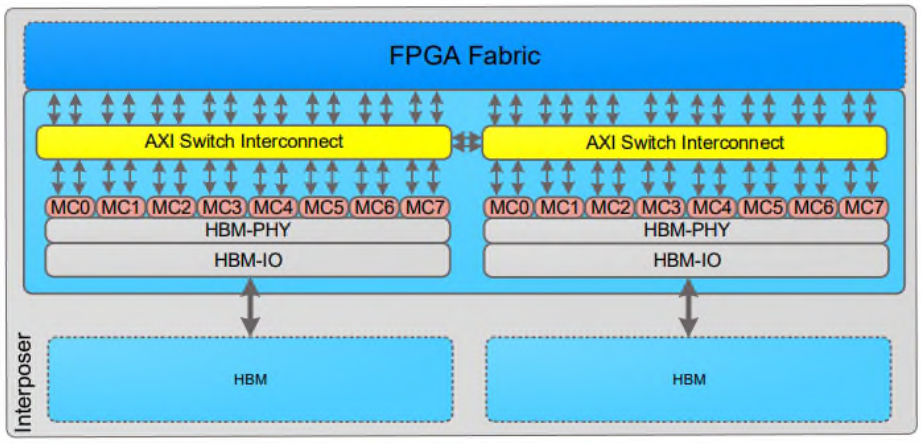


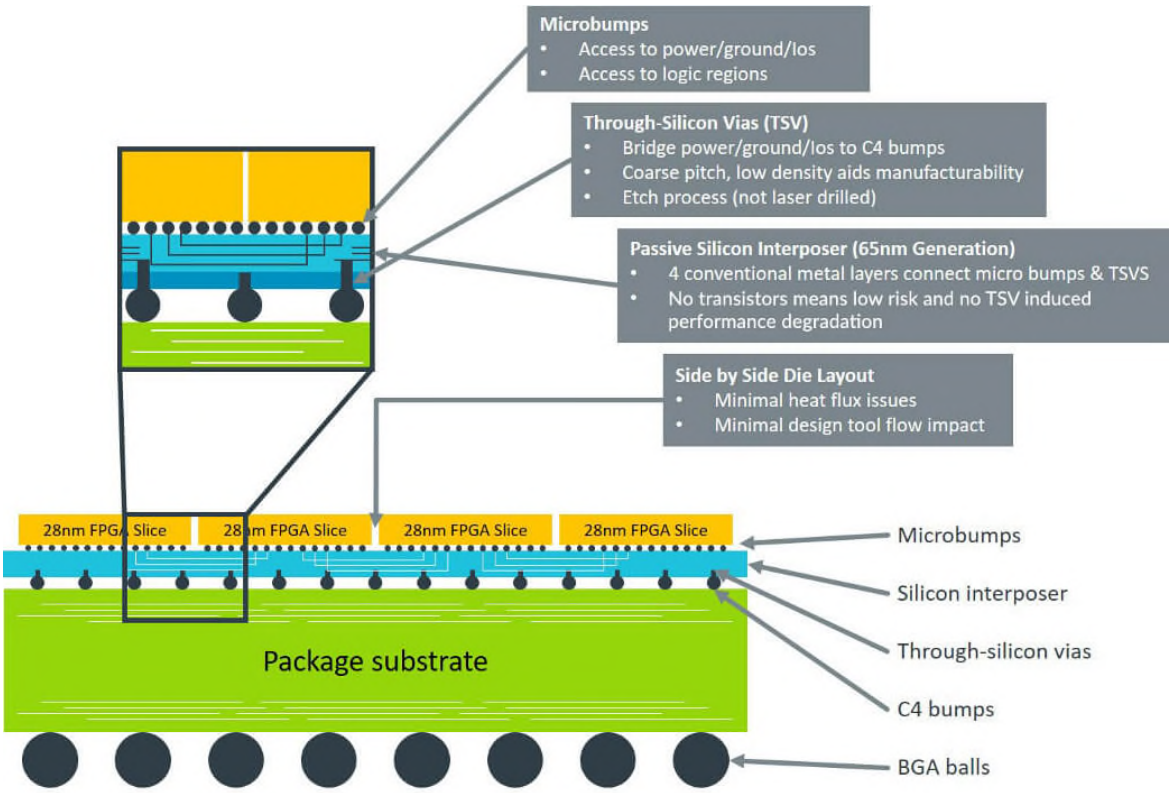
38. The ‘226 Accused Products accelerate the processing of data shared between the FGPA and other components, such as memory. Xilinx uses a silicon manufacturing process on which multiple die are set side-by-side and interconnected. SSI technology avoids the power and reliability issues. This technology, including the use of TSVs, provides massive bandwidth to accelerate processing without degrading or requiring additional power.

39. The ‘226 Accused Products also include extensive interconnect logic and block RAM memory for data processing and traffic management, including HBM which connect to FPGAs using TSVs.

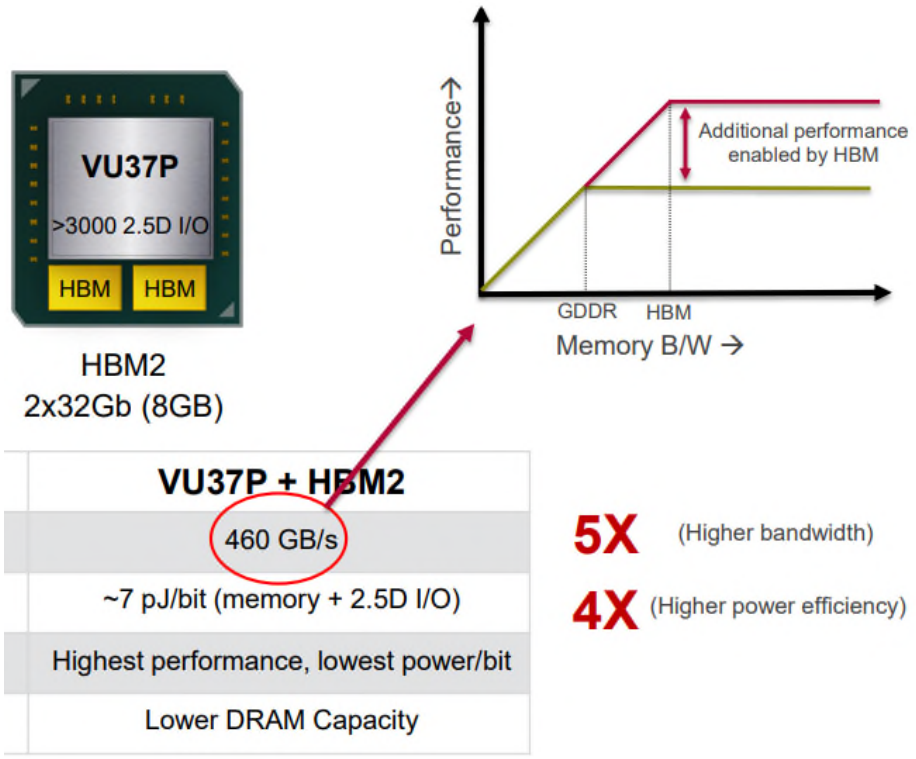


40. The FPGA and HBM die elements are electrically coupled and interconnected using interposers with TSVs.





41. The '226 Accused Products accelerate the processing of data shared between the microprocessor, such as the DSPs and the FGPA, such as the CLBs or with the HBM. Xilinx uses a silicon manufacturing process on which multiple die are set side-by-side and interconnected. SSI technology avoids the power and reliability issues. This technology including TSVs provides massive bandwidth to accelerate processing without degrading or requiring additional power.



See https://www.hotchips.org/wp-content/uploads/hc_archives/hc29/HC29.22-Tuesday-Pub/HC29.22.50-FPGA-Pub/HC29.22.530-Datacenter-16nm-Singh-Xilinx-VU37p-rev5.pdf

42. To the extent the ’226 Accused Products includes components or software owned or manufactured by third parties, the Accused Products still infringe the ’226 Patent because Defendant is vicariously liable for making, selling, offering for sale, and/or using the patented technology by controlling the design and operation of the ‘226 Accused Products that are made, used and sold. Further, Defendant derives a benefit from the manufacture and use of every element of the entire system

43. Defendant’s infringement of the ‘226 Patent injured Arbor in an amount to be proven at trial, but not less than a reasonable royalty.

COUNT II
(Indirect Infringement of the '226 Patent pursuant to 35 U.S.C. § 271(b))

44. Arbor repeats, realleges, and incorporates by reference, as if fully set forth herein, the allegations of the preceding paragraphs, as set forth above.

45. Defendant is on notice that the '226 Accused Products infringe the '226 Patent at least as of the service of this Complaint.

46. In addition to directly infringing the '226 Patent, Defendant knew or were willfully blind to the fact that they were inducing infringement under 35 U.S.C. § 271(b) by instructing, directing and/or imposing requirement to third parties on the manufacture and use of the '226 Accused Products.

47. Additionally, Defendant knew or were willfully blind to the fact that they were inducing infringement under 35 U.S.C. § 271(b) by instructing, directing and/or imposing requirement to third parties, including customers, manufactures, suppliers and agents, on the manufacture and use of the '226 Accused Products, either literally or under the doctrine of equivalents.

COUNT III
(Direct Infringement of the '214 Patent pursuant to 35 U.S.C. § 271(a))

48. Arbor repeats, realleges, and incorporates by reference, as if fully set forth herein, the allegations of the preceding paragraphs, as set forth above.

49. Defendant infringes at least Claim 1 of the '214 Patent in violation of 35 U.S.C. § 271(a).

50. Defendant's infringement is based upon literal infringement or, in the alternative, infringement under the doctrine of equivalents.

51. Defendant's acts of making, using, importing, selling, and offering for sale infringing products and services were without the permission, consent, authorization, or license of Arbor.

52. Defendant's infringement includes, the manufacture, use, sale, importation and offer for sale of Defendant's IC products that utilize processor modules that include multiple die elements electronically coupled through TSVs, including Xilinx's ICs with 3D Stacked Silicon Interconnects ("SSI") and HBM, which include Xilinx's Virtex FPGA, Virtex UltraScale FPGA, Virtex UltraScale+ FPGA, Kintex UltraScale FPGA, Kintex UltraScale+ FPGA ICs, and Virtex UltraScale+ HBM ICs (collectively, the "'214 Accused Products").

53. The '214 Accused Products practice the patented invention of the '214 Patent and Defendant infringes the '214 Patent because it makes, sells, offers for sale, and/or uses the Accused Products, which include processor modules that include multiple die elements electronically coupled through TSVs. Using the patented technology, the '214 Accused Products provide increased bandwidth and low latency operation.

54. The '214 Accused Products utilize 3D integrated circuits and SSI and are processing modules with a FPGA IC die element including programmable CLBs. Xilinx SSI technology uses the ASMBL architecture, which is a module structure that including FPGA building blocks as stacked tiles.

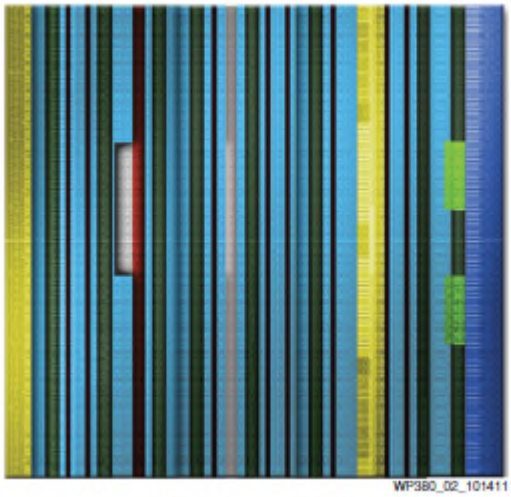


Figure 2: **Representation of an FPGA Built with ASMBL Architecture**

55. The ‘214 Accused Products include a microprocessor IC die element and memory arrays that are electrically coupled. Die components are electrically coupled using interposers with TSV to interconnect different logic regions.

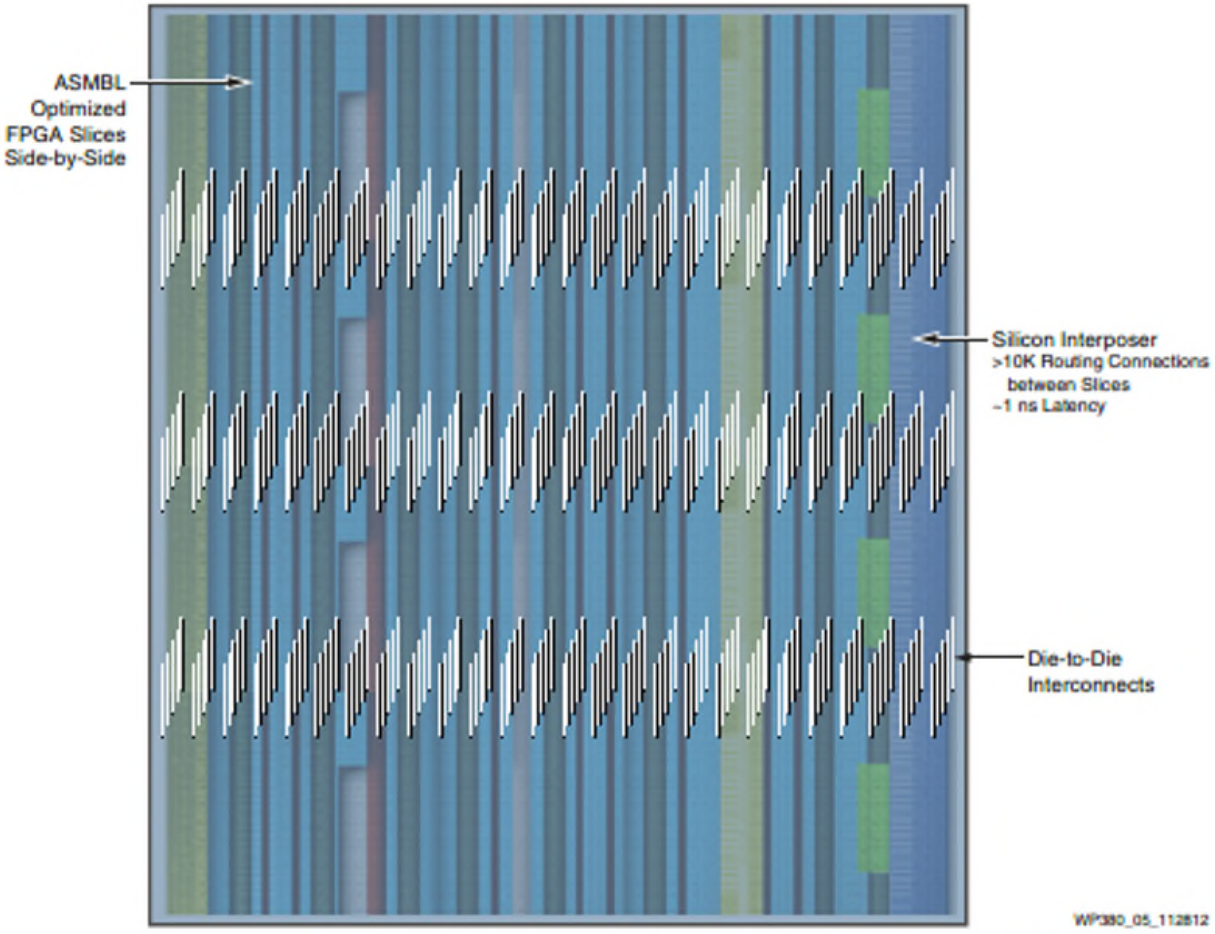
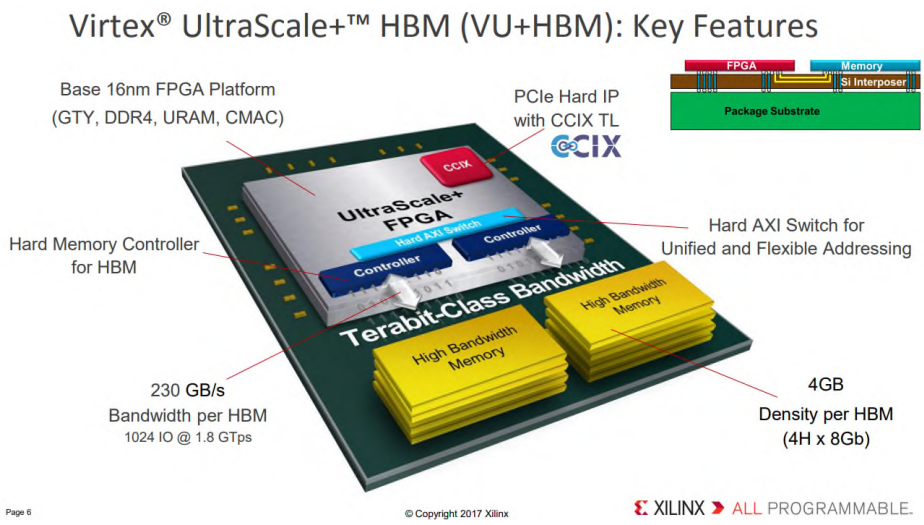
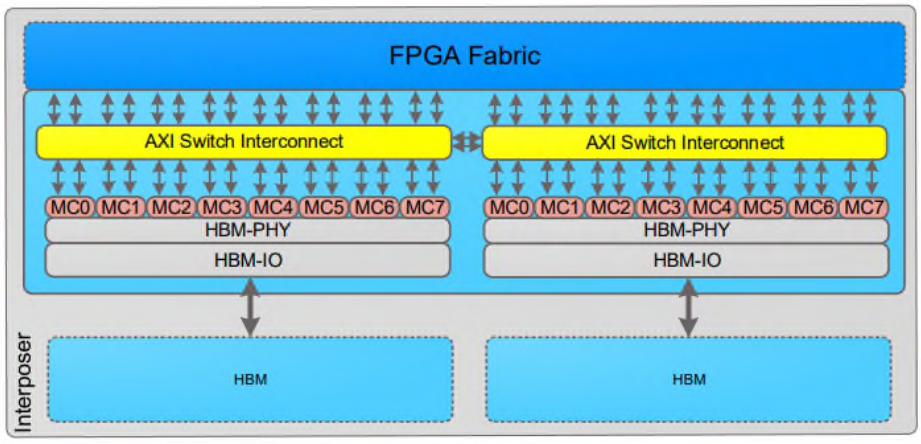


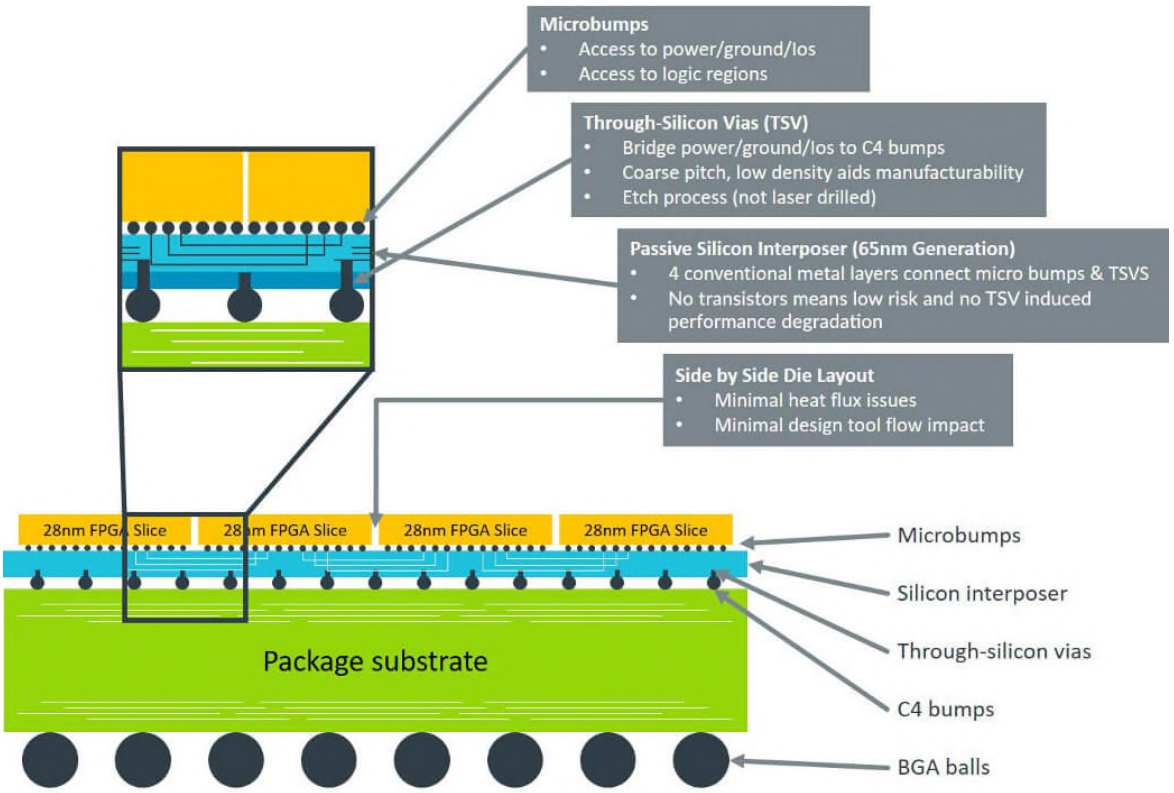
Figure 5: **"X-ray View" of a Virtex-7 FPGA Using SSI Technology**

56. The '214 Accused Products also include extensive interconnect logic and block RAM memory for data processing and traffic management, including HBM which connect to FPGAs using TSVs.

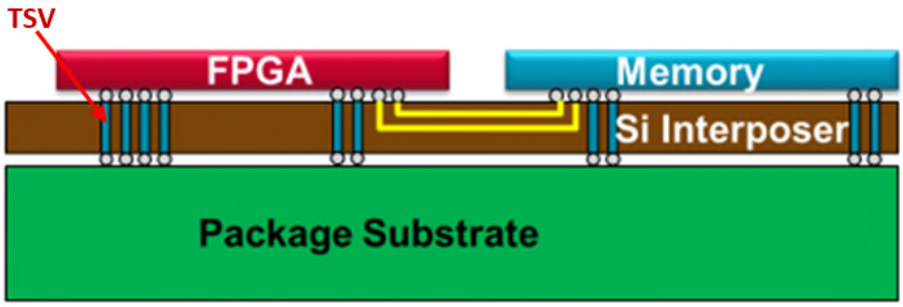


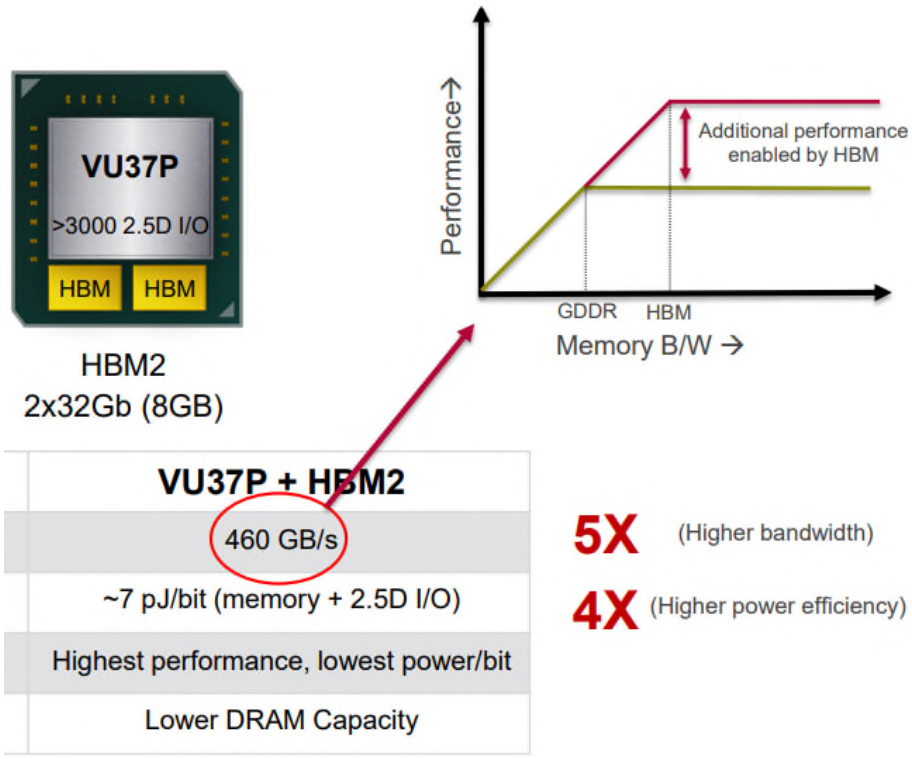
57. The FPGA and HBM die elements are electrically coupled and interconnected using interposers with TSVs.





58. The '214 Accused Products accelerate the processing of data shared between the microprocessor, such as the DSPs and the FGPA, such as the CLBs or with the HBM. Xilinx uses a silicon manufacturing process on which multiple die are set side-by-side and interconnected. SSI technology avoids the power and reliability issues. This technology including TSVs provides massive bandwidth to accelerate processing without degrading or requiring additional power.





59. To the extent the ’214 Accused Products includes components or software owned or manufactured by third parties, the Accused Products still infringe the ’214 Patent because Defendant is vicariously liable for making, selling, offering for sale, and/or using the patented technology by controlling the design and operation of the ‘214 Accused Products that are made, used and sold. Further, Defendant derives a benefit from the manufacture and use of every element of the entire system

60. Defendant’s infringement of the ‘214 Patent injured Arbor in an amount to be proven at trial, but not less than a reasonable royalty.

COUNT IV
(Indirect Infringement of the ‘214 Patent pursuant to 35 U.S.C. § 271(b))

61. Arbor repeats, realleges, and incorporates by reference, as if fully set forth herein, the allegations of the preceding paragraphs, as set forth above.

62. Defendant is on notice that the ‘214 Accused Products infringe the ‘214 Patent at least as of the service of this Complaint.

63. In addition to directly infringing the ‘214 Patent, Defendant knew or were willfully blind to the fact that they were inducing infringement under 35 U.S.C. § 271(b) by instructing, directing and/or imposing requirement to third parties on the manufacture and use of the ‘214 Accused Products.

64. Additionally, Defendant knew or were willfully blind to the fact that they were inducing infringement under 35 U.S.C. § 271(b) by instructing, directing and/or imposing requirement to third parties, including customers, manufactures, suppliers and agents, on the manufacture and use of the ‘214 Accused Products, either literally or under the doctrine of equivalents.

COUNT V
(Direct Infringement of the ‘951 Patent pursuant to 35 U.S.C. § 271(a))

65. Arbor repeats, realleges, and incorporates by reference, as if fully set forth herein, the allegations of the preceding paragraphs, as set forth above.

66. Defendant infringes at least Claim 1 of the ‘951 Patent in violation of 35 U.S.C. § 271(a).

67. Defendant’s infringement is based upon literal infringement or, in the alternative, infringement under the doctrine of equivalents.

68. Defendant’s acts of making, using, importing, selling, and offering for sale infringing products and services were without the permission, consent, authorization, or license of Arbor.

69. Defendant’s infringement includes, the manufacture, use, sale, importation and offer for sale of Defendant’s IC products that utilize processor modules that include multiple die

elements electronically coupled through TSVs, including Xilinx's ICs with 3D Stacked Silicon Interconnects ("SSI") and HBM, which include Xilinx's Virtex FPGA, Virtex UltraScale FPGA, Virtex UltraScale+ FPGA, Kintex UltraScale FPGA, Kintex UltraScale+ FPGA ICs, and Virtex UltraScale+ HBM ICs (collectively, the "'951 Accused Products").

70. The '951 Accused Products practice the patented invention of the '951 Patent and Defendant infringes the '951 Patent because it makes, sells, offers for sale, and/or uses the Accused Products, which include processor modules that include multiple die elements electronically coupled through TSVs. Using the patented technology, the '951 Accused Products provide increased bandwidth and low latency operation.

71. The '951 Accused Products utilize 3D integrated circuits and SSI and are integrated processing modules with a FPGA IC die element including programmable CLBs. Xilinx SSI technology uses the ASMBL architecture, which is a module structure that including FPGA building blocks.

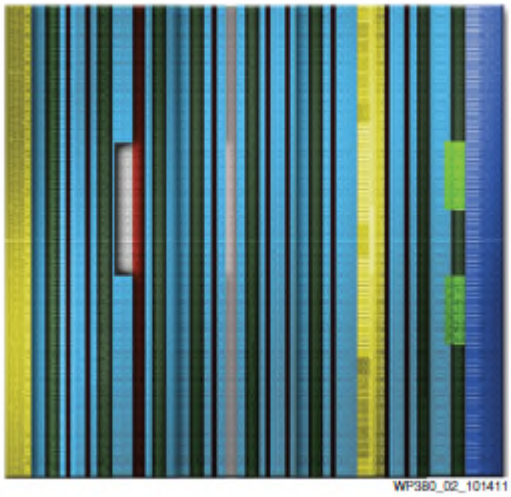
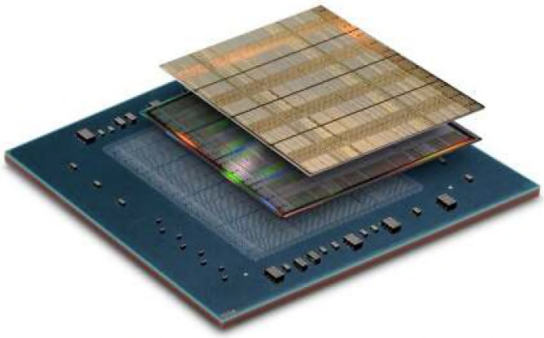


Figure 2: **Representation of an FPGA Built with ASMBL Architecture**

72. The '951 Accused Products include a microprocessor IC die element and memory arrays that are electrically coupled.



The Virtex-7 2000T has four FPGA dice in the same package

73. The ‘951 Accused Products also include extensive interconnect logic and block for data processing and traffic management using IC components, while maintaining current form factors and power footprints. Multiple die elements are electrically coupled and interconnected using interposers with TSVs and microbumps distributed in the IC. Die components are electrically coupled using interposers with TSV to interconnect different logic regions.

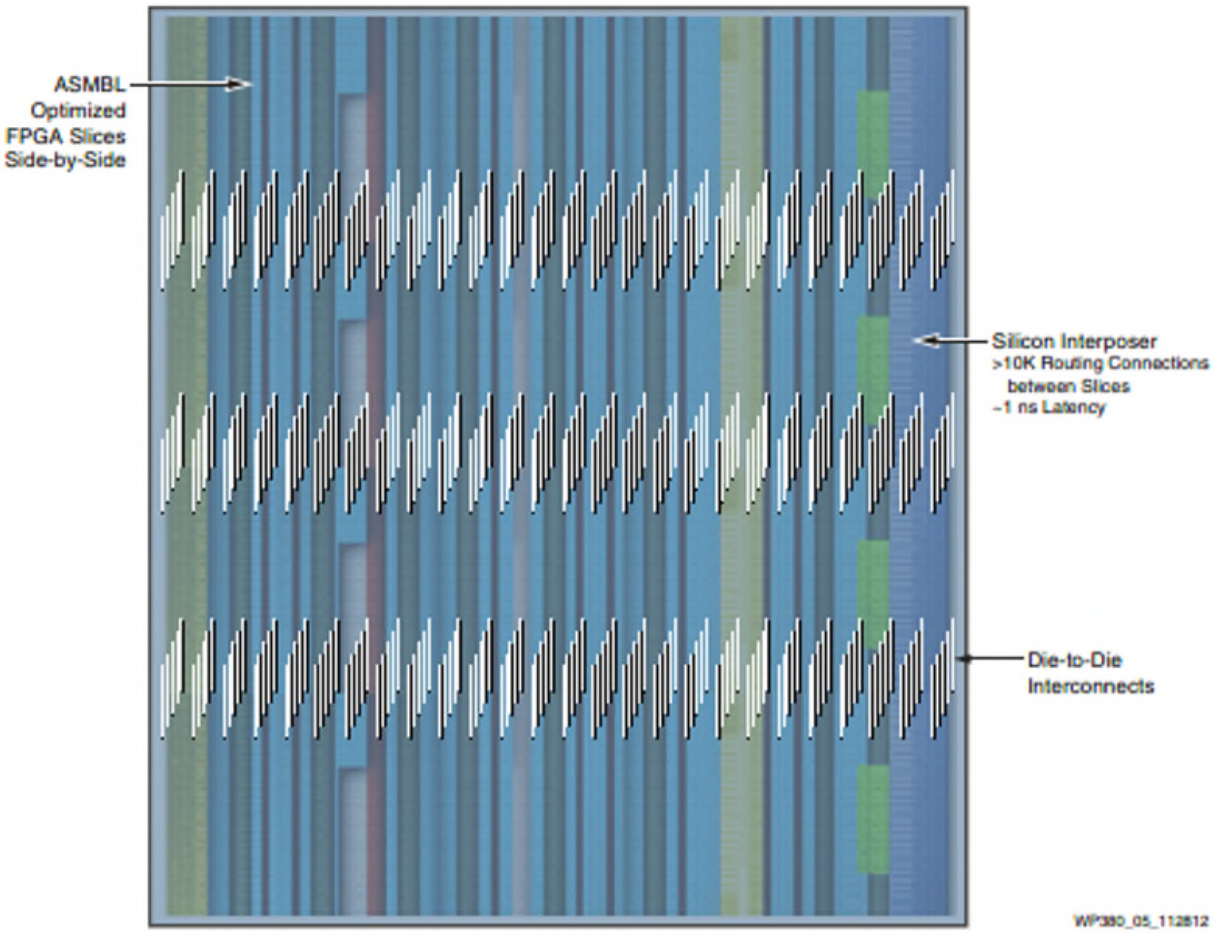
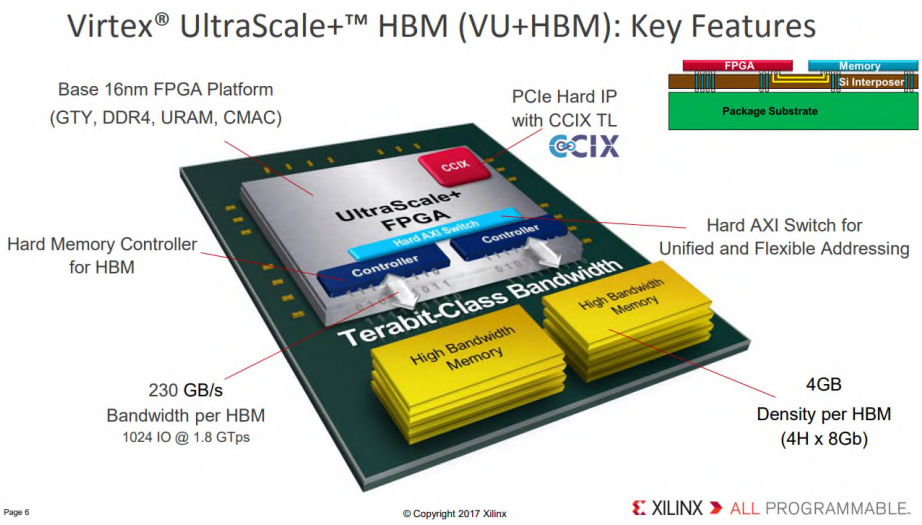
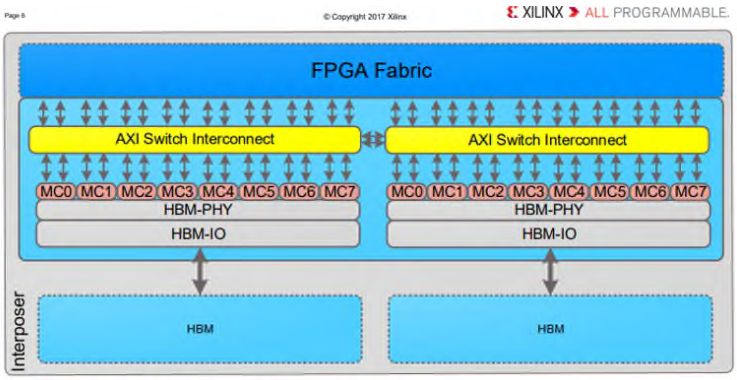


Figure 5: **"X-ray View" of a Virtex-7 FPGA Using SSI Technology**

74. The '951 Accused Products accelerate the processing of data shared between the microprocessor, such as the DSPs and the FGPA, such as the CLBs. Xilinx uses a silicon manufacturing process on which multiple die are set side-by-side and interconnected. SSI technology avoids the power and reliability issues. This technology including TSVs provides massive bandwidth to accelerate processing without degrading or requiring additional power.

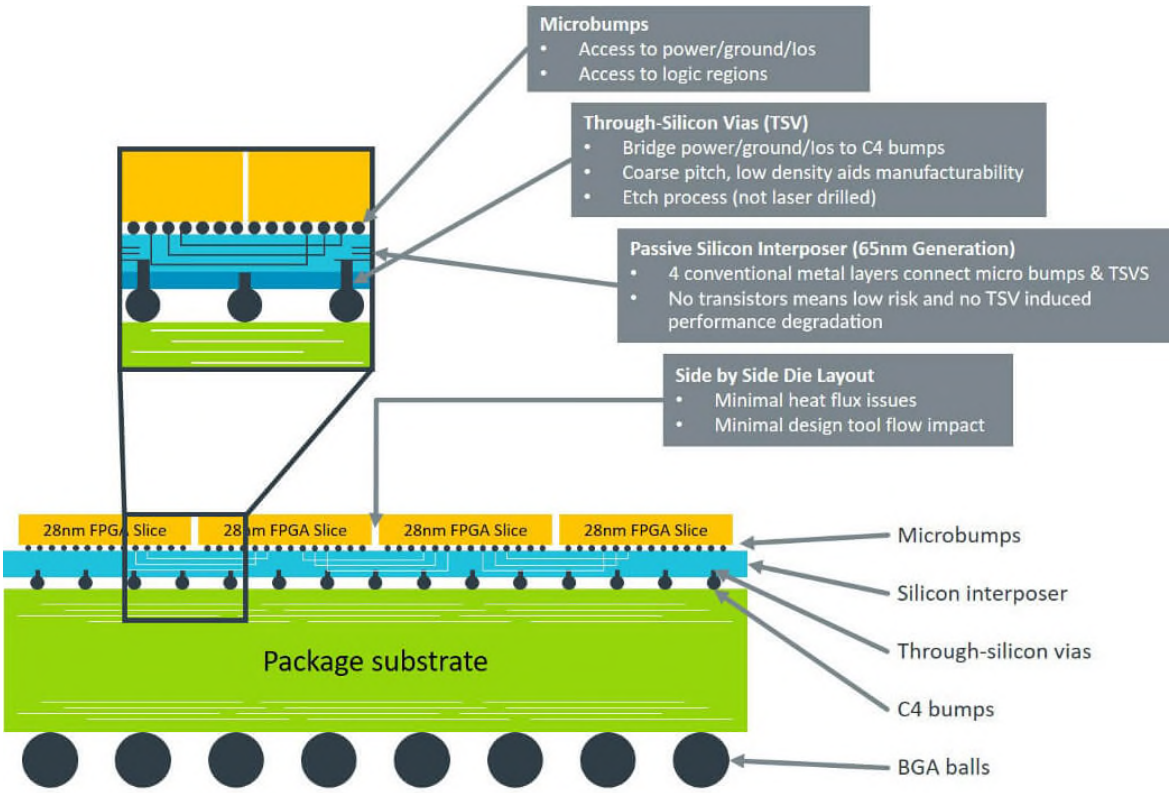
75. The '951 Accused Products also include extensive interconnect logic and block RAM memory for data processing and traffic management including HBM which connect to FPGA using TSVs.

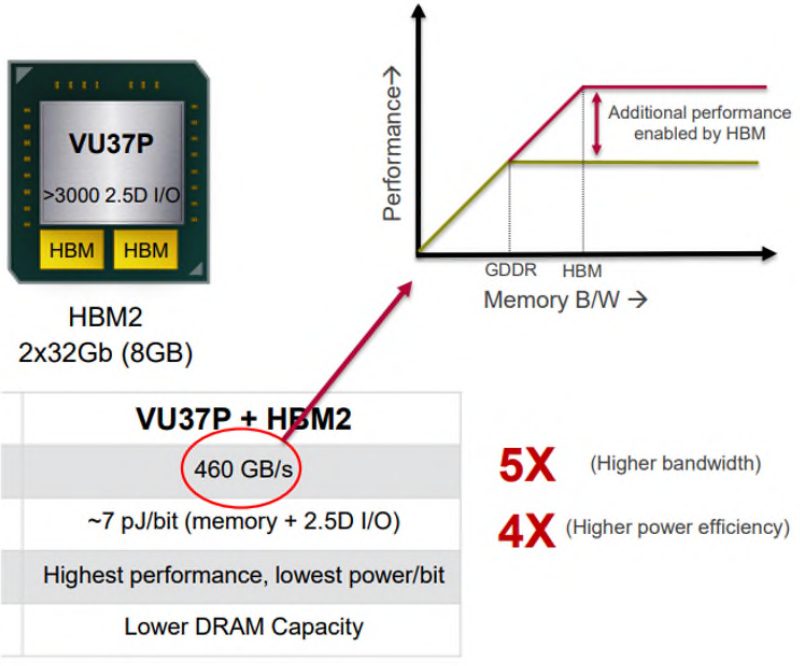




See https://www.hotchips.org/wp-content/uploads/hc_archives/hc29/HC29.22-Tuesday-Pub/HC29.22.50-FPGA-Pub/HC29.22.530-Datacenter-16nm-Singh-Xilinx-VU37p-rev5.pdf

76. The '951 Accused Products accelerate the processing of data shared between the microprocessor, such as the DSPs and the FGPA, such as the CLBs. Xilinx uses a silicon manufacturing process on which multiple die are set side-by-side and interconnected. SSI technology avoids the power and reliability issues. This technology provides massive bandwidth to accelerate processing without degrading or requiring additional power.





See https://www.hotchips.org/wp-content/uploads/hc_archives/hc29/HC29.22-Tuesday-Pub/HC29.22.50-FPGA-Pub/HC29.22.530-Datacenter-16nm-Singh-Xilinx-VU37p-rev5.pdf

77. To the extent the ’951 Accused Products includes components or software owned or manufactured by third parties, the Accused Products still infringe the ’951 Patent because Defendant is vicariously liable for making, selling, offering for sale, and/or using the patented technology by controlling the design and operation of the ‘951 Accused Products that are made, used and sold. Further, Defendant derives a benefit from the manufacture and use of every element of the entire system.

78. Defendant’s infringement of the ‘951 Patent injured Arbor in an amount to be proven at trial, but not less than a reasonable royalty.

COUNT VI
(Indirect Infringement of the ‘951 Patent pursuant to 35 U.S.C. § 271(b))

79. Arbor repeats, realleges, and incorporates by reference, as if fully set forth herein, the allegations of the preceding paragraphs, as set forth above.

80. Defendant is on notice that the ‘951 Accused Products infringe the ‘951 Patent at least as of the service of this Complaint.

81. In addition to directly infringing the ‘951 Patent, Defendant knew or were willfully blind to the fact that they were inducing infringement under 35 U.S.C. § 271(b) by instructing, directing and/or imposing requirement to third parties on the manufacture and use of the ‘951 Accused Products.

82. Additionally, Defendant knew or were willfully blind to the fact that they were inducing infringement under 35 U.S.C. § 271(b) by instructing, directing and/or imposing requirement to third parties, including customers, manufactures, suppliers and agents, on the manufacture and use of the ‘951 Accused Products, either literally or under the doctrine of equivalents.

COUNT VII
(Direct Infringement of the ‘035 Patent pursuant to 35 U.S.C. § 271(a))

83. Arbor repeats, realleges, and incorporates by reference, as if fully set forth herein, the allegations of the preceding paragraphs, as set forth above.

84. Defendant infringes at least Claim 23 of the ‘035 Patent in violation of 35 U.S.C. § 271(a).

85. Defendant’s infringement is based upon literal infringement or, in the alternative, infringement under the doctrine of equivalents.

86. Defendant’s acts of making, using, importing, selling, and offering for sale infringing products and services were without the permission, consent, authorization, or license of Arbor.

87. Defendant’s infringement includes the manufacture, use, sale, importation and offer for sale of Defendant’s IC products that utilize FPGA processor modules that include multiple die elements electronically coupled through TSVs, including Xilinx’s IC with 3D Stacked Silicon Interconnects (“SSI”) and HBM, and which include Xilinx’s Virtex FPGA, Virtex UltraScale FPGA, Virtex UltraScale+ FPGA, Kintex UltraScale FPGA, Kintex UltraScale+ FPGA ICs, and Virtex UltraScale+ HBM ICs (collectively, the “’035 Accused Products”).

88. The ’035 Accused Products practice the patented invention of the ’035 Patent and Defendant infringes the ’035 Patent because it makes, sells, offers for sale, and/or uses the ‘035 Accused Products, which include FPGA processor modules that include multiple die elements electronically coupled through TSVs. Using the patented technology, the ‘035 Accused Products provide increased bandwidth and low latency operation.

89. The ‘035 Accused Products utilize 3D integrated circuits and SSI and are integrated processing modules with a FPGA IC die element including programmable CLBs. Xilinx SSI technology uses the ASMBL architecture, which is a module structure that including FPGA building blocks as stacked tiles.

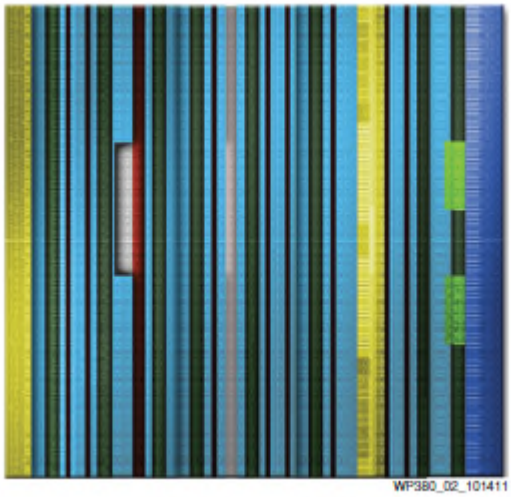
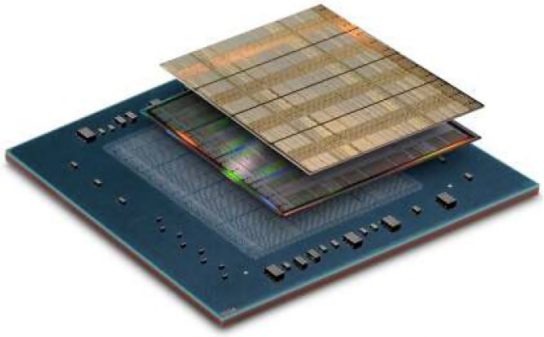


Figure 2: **Representation of an FPGA Built with ASMBL Architecture**

90. The ‘035 Accused Products include a microprocessor IC die element and memory arrays that are electrically coupled.



The Virtex-7 2000T has four FPGA dice in the same package

91. The ‘035 Accused Products also include extensive interconnect logic and block for data processing and traffic management using IC components, such as FPGAs, while maintaining current form factors and power footprints. Multiple die elements are electrically

coupled and interconnected using interposers with TSVs and microbumps distributed in the IC. Die components are electrically coupled using interposers with TSV to interconnect different logic regions.

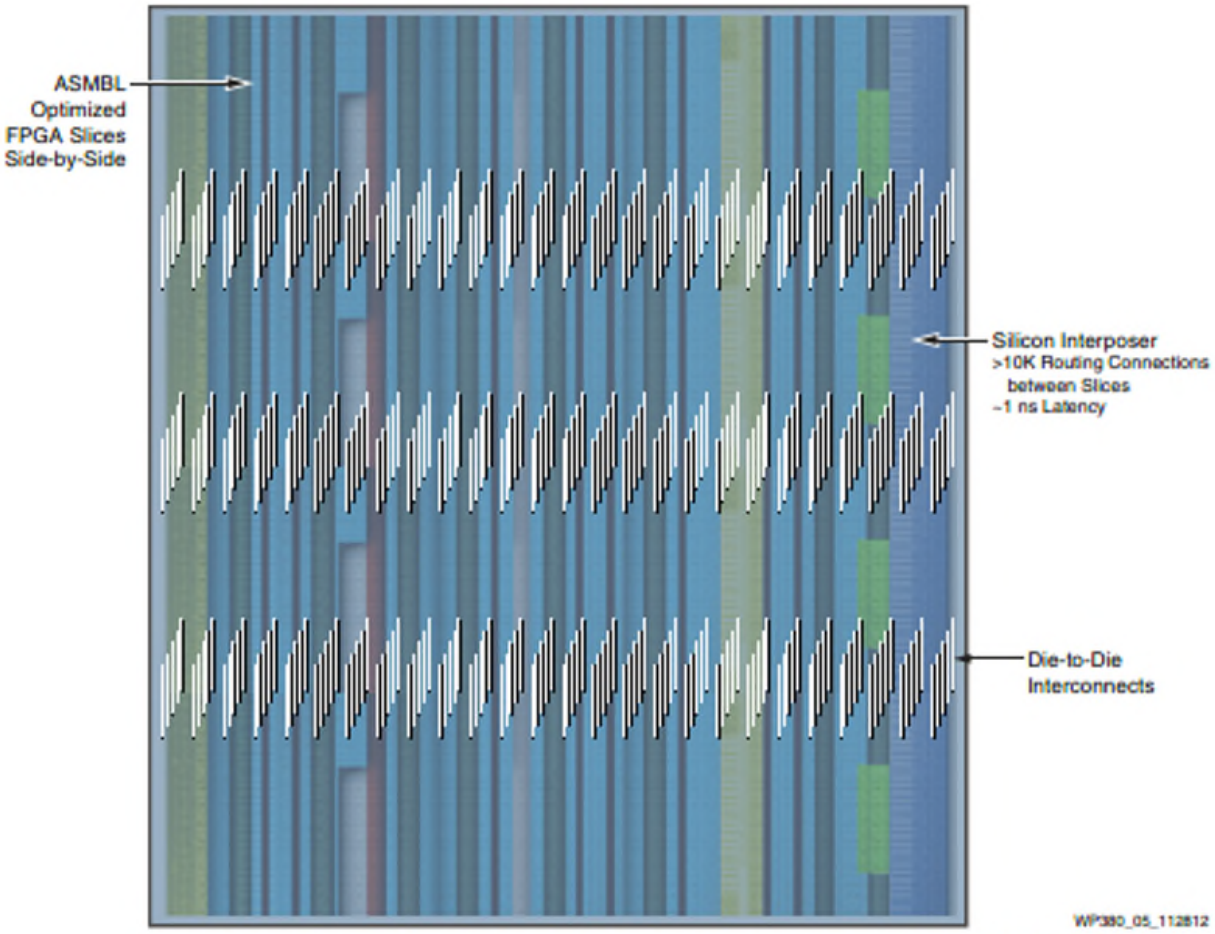
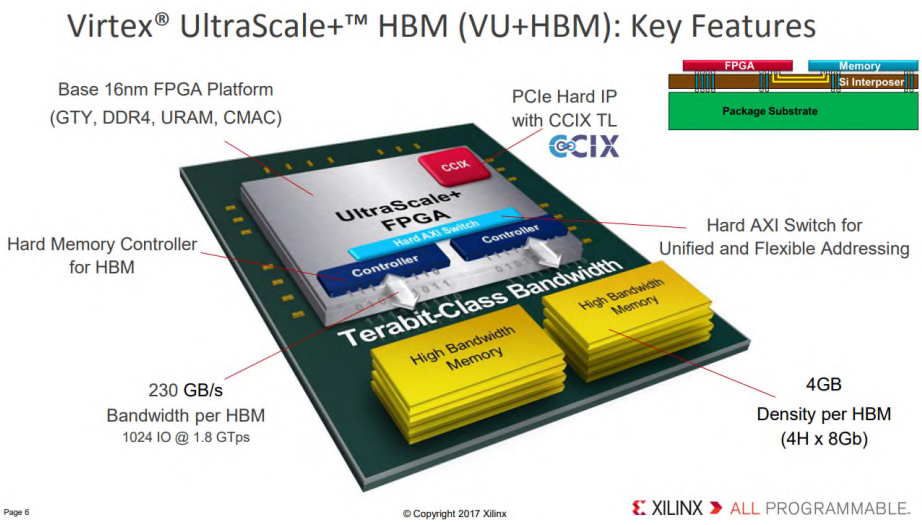
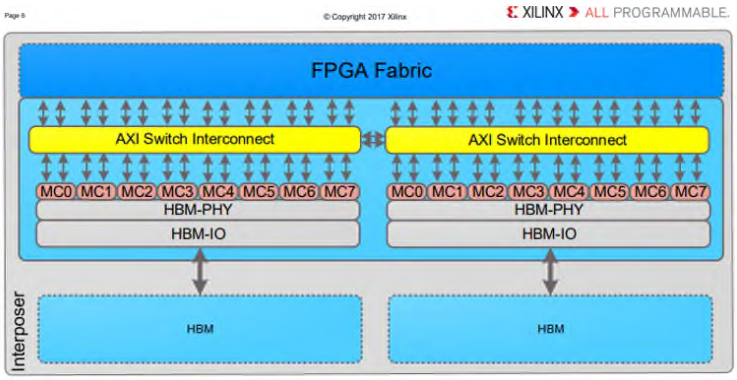


Figure 5: **"X-ray View" of a Virtex-7 FPGA Using SSI Technology**

92. The '035 Accused Products also include extensive interconnect logic and block RAM memory for data processing and traffic management including HBM which connect to FPGA using TSVs.





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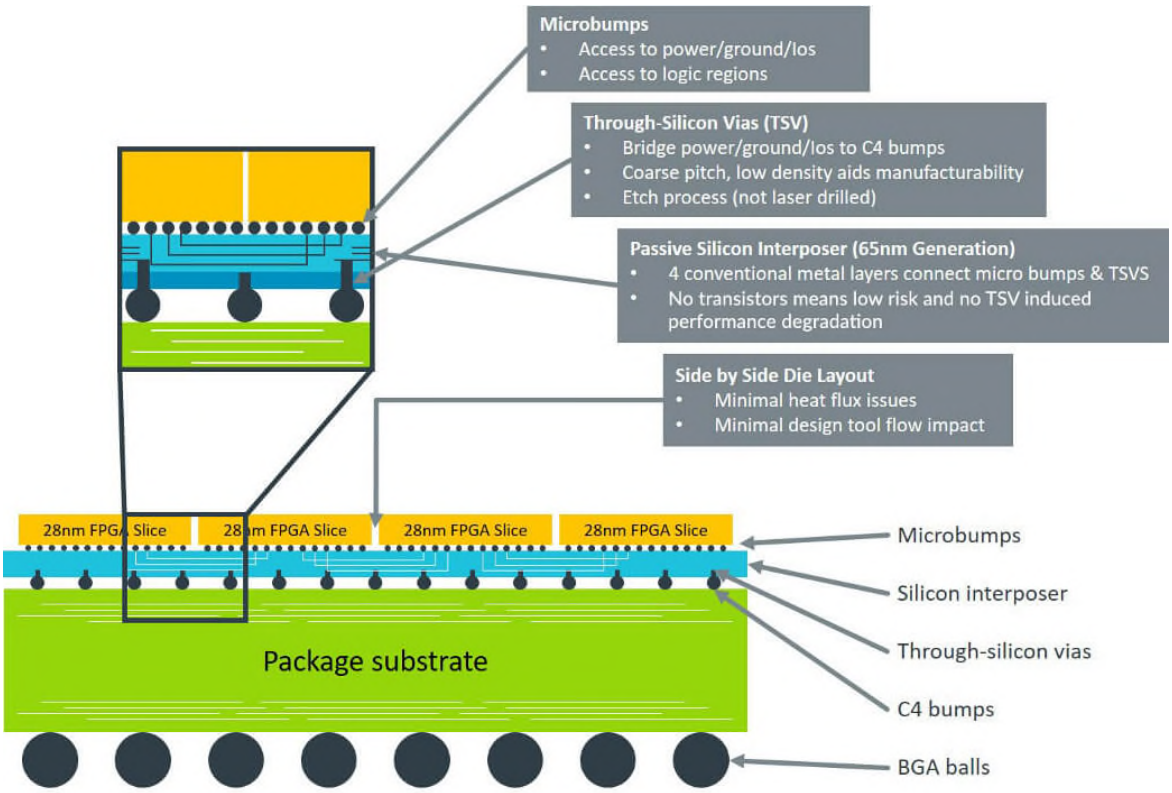
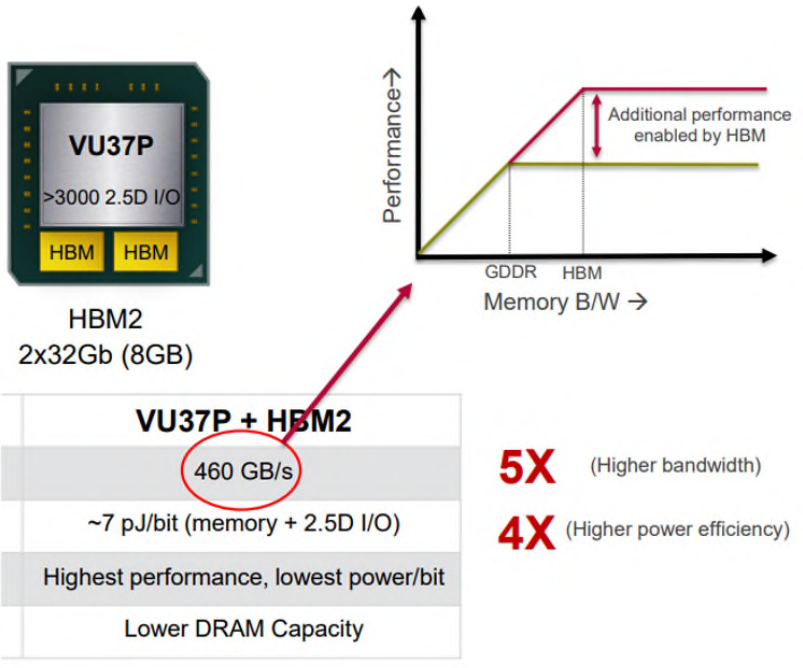
93. The '035 Accused Products accelerate the processing of data shared between the microprocessor, such as the DSPs and the FGPA, such as the CLBs. Xilinx uses a silicon manufacturing process on which multiple die are set side-by-side and interconnected. SSI technology avoids the power and reliability issues. This technology provides massive bandwidth to accelerate processing without degrading or requiring additional power.





See https://www.hotchips.org/wp-content/uploads/hc_archives/hc29/HC29.22-Tuesday-Pub/HC29.22.50-FPGA-Pub/HC29.22.530-Datacenter-16nm-Singh-Xilinx-VU37p-rev5.pdf

94. To the extent the ’035 Accused Products includes components or software owned or manufactured by third parties, the ‘035 Accused Products still infringe the ’035 Patent because Defendant is vicariously liable for making, selling, offering for sale, and/or using the patented technology by controlling the design and operation of the ‘035 Accused Products that are made, used and sold. Further, Defendant derives a benefit from the manufacture and use of every element of the entire system.

95. Defendant’s infringement of the ‘035 Patent injured Arbor in an amount to be proven at trial, but not less than a reasonable royalty.

COUNT VIII
(Indirect Infringement of the ‘035 Patent pursuant to 35 U.S.C. § 271(b))

96. Arbor repeats, realleges, and incorporates by reference, as if fully set forth herein, the allegations of the preceding paragraphs, as set forth above.

97. Defendant is on notice that the ‘035 Accused Products infringe the ‘035 Patent at least as of the service of this Complaint.

98. In addition to directly infringing the ‘035 Patent, Defendant knew or was willfully blind to the fact that it was inducing infringement of the ‘035 Patent under 35 U.S.C. § 271(b) by instructing, directing and/or imposing requirement to third parties on the manufacture and use of the ‘035 Accused Products.

99. Additionally, Defendant knew or was willfully blind to the fact that it was inducing infringement of the ‘035 Patent under 35 U.S.C. § 271(b) by instructing, directing and/or imposing requirement to third parties, including customers, manufactures, suppliers and agents, on the manufacture and use of the ‘035 Accused Products, either literally or under the doctrine of equivalents.

PRAYER FOR RELIEF

WHEREFORE, Arbor prays for judgment and relief as follows:

A. An entry of judgment holding that Defendant infringed the ‘226, ‘214, ‘951, and ‘035 Patents; induced infringement of the ‘226, ‘214, ‘951, and ‘035 Patents.

B. An award to Arbor of such past damages, not less than a reasonable royalty, as it shall prove at trial against Defendant that is adequate to fully compensate Arbor for Defendant’s infringement of the ‘‘226, ‘214, ‘951, and ‘035 Patents;

C. A finding that this case is “exceptional” and/or an award to Arbor of its costs and reasonable attorneys’ fees, as provided by 35 U.S.C. § 285;

D. An accounting of all infringing sales and revenues, together with post judgment interest and prejudgment interest from the first date of infringement of the ‘226, ‘214, ‘951, and ‘035 Patents; and

E. Such further and other relief as the Court may deem proper and just.

DEMAND FOR JURY TRIAL

Arbor demands a jury trial on all issues so triable.

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Dated: October 18, 2019
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